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EXAMINER	
KHOO, FOONG LIN	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,728	WILLIAMS ET AL.	
	Examiner	Art Unit	
	F. Lin Khoo	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/01/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 12-18, 20-22, 23-25, 26-28, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Giacopelli et al. (U.S. Patent No. 4,893,304).

Regarding Claim 1, Giacopelli et al. discloses a method comprising: buffering a set of items, the set of items including a first set of items and a second set of items (Fig. 1A (element 54), Fig. 1B (element 18); col 3, lines 36-50; col 5, lines 31-37; col 6, line 52 through col 7, line 8). The first set of items are associated with selector cells (element 38, 40-1 through 40-N) outputs $e_{1b},\ldots a_{Nb}$ transmitted to the Banyan networks 14a, 14b for routing to particular output port controller. The second set of items are associated with outputs from selector cells (element 38, 40-1 through 40-N) designated as $e_{1a}, \ldots e_{Ma}$ to inputs $a_1,..a_m$ forming the recirculation loops (Fig. 1A, element 30). Buffering of first set of items and second set of items occur in Fig. 1A (element 54), Fig. 1B (element 18). Note: The first set and second set of items are any packets destined for transmission over an available output path configured in a plurality of configurations in the Banyan networks. Therefore, the terms first set and second set are interpreted interchangeably);

forwarding the first set of items over a set of paths in a first configuration (Fig. 1A and 1B, col 5, lines 31-37. Connection path h1 to p1 to output port 18-1 from Banyan network 14a is associated with forwarding the first set of items over a set of paths in a first configuration);

reconfiguring the set of paths into a second configuration (Fig. 1A and 1B, col 5, lines 31-37. Connection path l1 to q1 to output port 18-1 from Banyan network 14b is associated with reconfiguring the set of paths into a second configuration); and

forwarding one or more items in the second set of items over the set of paths in the second configuration (Fig. 1A and 1B, col 5, lines 31-37; col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers and packets to be recirculated. The second set of items related to packets that have been recirculated, when identified by the trapping network to be routed to the output port controllers, is associated with forwarding one or more items in the second set of items over the set of paths in the second configuration).

Regarding Claim 2, Giacopelli et al. discloses wherein said reconfiguring the set of paths into the second configuration is based on a random indication (Fig. 1(element 12) and Fig. 2; col 5, lines 3-30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains two sub-fields, service priority field (SP) and switch priority (PR). Sorting the SP and PR (a count of number of time slots packet has been delayed) fields is equivalent to reconfiguring the set of paths into the second configuration based on a random

indication which is provided by the randomness of both the service priority and switch priority of the packets).

Regarding Claim 3, Giacopelli et al. discloses wherein said reconfiguring the set of paths into the second configuration includes modifying a reference value (col 5, lines 19-23. The switch priority (PR) sub-field in the priority field has an initial value and for every slot a packet is delayed, the PR-subfield is decremented. The initial value and decrementing of the PR-subfield are associated with reconfiguring the set of paths into the second configuration based on modifying a reference value).

Regarding Claim 4, Giacopelli et al. discloses placing the second set of items in a recirculation buffer (Fig. 1A and 1B, element 30 and element 54; col 6, line 52 through col 7, line 8. The second set of items are associated with outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} placed into shift registers (element 52) forming the recirculation loops (Fig. 1A, element 30). Note: A recirculation buffer is equivalent to a shift register in the recirculation loop).

Regarding Claim 5, Giacopelli et al. discloses retrieving said one or more items in the second set of items from the recirculation buffer (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers and packets to be recirculated. The recirculated packets placed in the shift register (element 52) when

identified by the trapping network to be routed to the output port controllers is equivalent to retrieving one or more items in the second set of items from the recirculation buffer).

Regarding Claim 6, Giacopelli et al. discloses identifying a status condition associated with each particular path of the set of paths corresponding to each of the items in the second set of items (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 3; col 5, line 55 through col 6, line 6. A trap bit in the packet is set if the compared destination addresses are equal and the packet is to be recirculated. The trap bit is not set if the compared destination addresses are not equal and the packet is to exit to an output port controller via a banyan network 14. Setting the trap bit to determine if the packet is to be recirculated or transmitted to an output port controller via a Banyan network 14 is identifying a status condition associated with each particular path of the set of paths corresponding to each of the items in the second set of items).

Regarding Claim 7, Giacopelli et al. discloses wherein said identifying the status condition includes referencing one or more data structures (col 6, lines 25-34; col 7, lines 3-25. The exiting packets (packets sent to the Banyan networks, Fig. 1B, 14a and 14b) are repacked into an ascending list by destination address without any gaps between them. An inverse perfect shuffle wiring pattern 42 connects the outputs e_{1b}, e_{2b}, . . e_{Nb} to the banyan networks. This wiring pattern divides the sorted list of packets present at the outputs e_{1b}, e_{2b}, . . e_{Nb} into two separate but sorted lists having a unique set of destination addresses. The path connection to the Banyan networks with unique

set of destination addresses into two separate sorted lists is associated with identifying the status condition which includes referencing one or more data structures. Note: The data structure is the list linking the path connection with the destination addresses).

Regarding Claim 8, Giacopelli et al. discloses identifying the status each path of the set of paths (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 3; col 5, line 55 through col 6, line 6. A trap bit in the packet is set if the compared destination addresses are equal and the packet is to be recirculated. The trap bit is not set if the compared destination addresses are not equal and the packet is to exit to an output port controller via a banyan network 14. Setting the trap bit to determine if the packet is to be recirculated or transmitted to an output port controller via a Banyan network 14 is associated with identifying the status each path of the set of paths).

Regarding Claim 9, Giacopelli et al. discloses wherein the set of items includes packets or identifiers of packets (Fig. 2 and Fig. 9, col 5, lines 3-5; col 11, lines 5-25).

Regarding Claim 10, Giacopelli et al. discloses wherein said reconfiguring the set of paths into the second configuration includes physically or logically adjusting the paths (col 10, line 64 through col 11, line 4).

Regarding Claim 12, Giacopelli et al. discloses a method comprising:

identifying a random index (Fig. 1(element 12) and Fig. 2; col 5, lines 3-30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains two sub-fields, service priority field (SP) and switch priority (PR) (PR is a count of number of time slots packet has been delayed) fields. The switch priority (PR) is identified to be a random index);

repeating for each first particular packet of a first set of packets stored in a recirculation buffer (Fig. 1A, element 30 and 52 The recirculating packets placed in the shift register (element 52. Note: a shift register is equivalent to a recirculation buffer) in the recirculation loop (element 30) arrive at inputs a_1, ...a_M of the Batcher network 12. The recirculating packets are subjected to sorting over the priority field for packets addressed to the same destination and therefore the process is repeated using the switch priority (PR) identified as a random index):

determining whether the first particular packet can be sent over a first particular path of a plurality of paths, the first particular path identified based on the random index and a path occupancy (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 2, Fig. 3; col 5, lines 3-30; col 5, line 55 through col 6, line 6. The trap cell uses a comparator circuit to determine whether a particular packet can be sent over a particular path of a plurality of paths, the particular path identified based on the random index (switch priority (PR)) and a path occupancy (activity bit (A). Note: activity bit when set to "0" represents idle packet (recirculated packet) and when set to "1" is active packet (exiting packet equivalent to path occupancy))) and

causing said first particular packet to be sent over the first particular path or to remain in the recirculation buffer based on the result of said determining whether the first particular packet can be sent (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated); and

repeating to cause packets to be sent over a set of remaining paths of the plurality of paths not currently sent a packet from the recirculation buffer (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated. The recirculated packets placed in the shift register (element 52) when identified by the trapping network to be routed to the output port controllers (i.e., compared destination address are not equal, the trap bit in the packet is not set and the packet is to exit to an output port controller via a Banyan network 14)):

determining whether a second particular packet of a second set of received packets can be sent over a second particular path of a plurality of paths, the second particular path identified based on the random index and the path occupancy (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 2, Fig. 3; col 5, lines 3-30; col 5, line 55 through col 6, line 6. The trap cell uses a comparator circuit to determine whether a particular packet can be sent over a particular path of a plurality of paths, the particular path identified based on the random index (switch priority (PR)) and a path occupancy (activity bit (A). Note: activity bit when set to "0" represents idle packet (recirculated

packet) and when set to "1" is active packet (exiting packet equivalent to path occupancy))); and

causing said second particular packet to be sent over the second particular path or to remain in the recirculation buffer based on the result of said determining whether the second particular packet can be sent (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated).

Regarding Claim 13, Giacopelli et al. discloses the method of claim 12 repeated once for each packet time (Fig. 7, col 9, line 67 through col 10, line 40. The network 80 dynamically allocates inputs between newly arriving packets and recirculating packets at each packet time slot).

Regarding Claim 14, Giacopelli et al. discloses wherein the path occupancy is determined based on a number of paths over which the first particular packet or the second particular packet is caused to be sent in a current packet time (Fig. 6, Fig. 7, col 9, line 52 through col 10, line 40. All newly arriving packets at each input port controller are delayed for a period in excess of one packet slot. This provides time for an input port controller to decide in time slot T if it will be idle during the time slot T+2. If an input port controller will be idle during time slot T+2, then it serves as an access point for a recirculating packet. In such a case, the input port controller submits an active steering packet to the concentrator 92 that will be paired with a recirculating packet to provide a

routing header that returns the recirculating packet to the input port controller that issued the steering packet. The input port controller that receives the recirculating packet, will then resubmit the recirculating packet to the network 82 in the T+2 time slot. An input port controller that will not be idle during the packet time slot T+2 generates an idle steering packet during the packet slot T as indicated by an activity bit being set to zero. This process is equivalent to packet sent in a current packet time).

Regarding Claim 15, Giacopelli et al. discloses wherein the current packet time corresponds to a round of sending one packet over each of the plurality of paths (Fig. 6, Fig. 7, col 9, line 25 through col 10, line 40. The network 80 dynamically allocates inputs between newly arriving packets and recirculating packets and routes either packets to the output port controller (element 18-1 through 18-N) via the network 82 in the current packet time slot).

Regarding Claim 16, Giacopelli et al. discloses wherein each of the plurality of paths corresponds to a different physical plane of a packet switching system (Fig. 1B, element 14a and 14b. Connections from input f_1 to h_1 and f_3 to h_2 in Banyan network 14a (one switch plane) and input g_1 to l_1 and g_3 to l_2 in Banyan network 14b (another switch plane) is associated with each of the plurality of paths corresponding to a different physical plane of a packet switching system).

Regarding Claim 17, Giacopelli et al. discloses wherein the plurality of paths does not include all of the planes of a packet switching system (Fig. 1B, element 14a and 14b; col 5, line 55 through col 6, line 6. When all of the paths in the Banyan networks 14a and 14 b are occupied (the activity bit set to "1") in the transmission of packets, then the packets are recirculated via the recirculation loop (Fig. 1B, element 30) and placed in the shift register (Fig. 1A, element 52). The trap cell network (Fig. 1A, element 32) determines that if the compared destination addresses are equal the packets are recirculated and therefore this corresponds to the plurality of paths which does not include all of the planes of a packet switching system).

Regarding Claim 18, Giacopelli et al. discloses wherein the plurality of paths includes all of the planes of a packet switching system (Fig. 1B, element 14a and 14b; col 5, line 55 through col 6, line 6. When all of the paths in the Banyan networks 14a and 14b are not occupied (the activity bit set to "0") in the transmission of packets, the trap cell network (Fig. 1A, element 32) determines that compared destination addresses are not equal, the packets are forwarded to output port controllers via the Banyan networks 14a and 14b. This is associated with the plurality of paths including all of the planes of a packet switching system).

Regarding Claim 20, Giacopelli et al. discloses an apparatus for forwarding information over a plurality of paths, the apparatus comprising:

a recirculation buffer to store a first set of packets (Fig. 1A, element 52; col 6, lines 63-66. A shift register for queuing is a recirculation buffer to store packets);

a random index generator to generate a random index (Fig. 1A, element 12, Fig. 2; col 4, line 43 through col 5, line 30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains two sub-fields, service priority field (SP) and switch priority (PR) (a count of number of time slots packet has been delayed). The Batcher network 12 is a random index generator to generate a random index based on the sorting of the SP and PR fields which is a random process);

an input to receive a second set of packets (Fig. 1A , element 16-M+1(input port controller); col 4, lines 28-42); and

control logic coupled to the recirculation buffer, the random index generator, the set of paths, and the input (Fig. 1A , 1B, Fig. 6, element 80 (conflict resolution and routing); col 9, lines 39-49. The conflict resolution and routing device is a control logic consisting of elements 12 (Batcher network), element 32 (trap cell network), element 36 (concentrator), element 38 (selector cell network) and elements 14a, 14b (Banyan network) and is coupled to the recirculation buffer (element 52 via loop 30), random index generator (Batcher network), the set of paths (Banyan network) and the input (input port controller));

wherein the control logic attempts to forward a packet over each of the plurality of paths each packet time from the first and second sets of packets with preference given to the first set of packets (Fig. 5; col 7, line 51 through col 9, line 2; Packets are given access

to the recirculation loops based on priority, not destination address, so that the lowest priority packets are the first to be lost at overload. To accomplish this, the packets are recorded before the recirculation. A packet switch 110 for carrying out such reordering is shown in FIG. 5 and attempts to forward a packet over each of the plurality of paths each packet time from the first and second sets of packets with preference given to the first set of packets),

wherein a particular path for a particular packet is determined based on the random index and an occupancy rate of the plurality of paths during a particular packet time (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 2, Fig. 3; col 5, lines 3-30; col 5, line 55 through col 6, line 6. The trap cell uses a comparator circuit to determine whether a particular packet can be sent over a particular path of a plurality of paths, the particular path identified based on the random index (switch priority (PR)) and a path occupancy (activity bit (A). Note: activity bit when set to "0" represents idle packet (recirculated packet) and when set to "1" is active packet (exiting packet equivalent to path occupancy))), and

wherein a particular packet remains or is added to the recirculation buffer if it is not sent over one of the plurality of paths during the particular packet time (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated).

Regarding Claim 21, Giacopelli et al. discloses wherein the particular packet is not sent during the particular packet time if a destination of the particular packet is not reachable over its corresponding the particular path (Fig. 1A and 1B, element 30, element 54, element 34-3 through 34-N; col 5, line 55 through col 6, line 3; col 6, line 52 through col 7, line 8. The trapping network (Fig. 1A, element 32) identifies packets to be recirculated when the compared destination addresses are equal and are not sent to the output port controller via the Banyan network. The outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} are packets not sent if the destination is not available for the packets).

Regarding Claim 22, Giacopelli et al. discloses comprising a storage mechanism coupled to the control logic to indicate whether the destination is reachable over the particular path (Fig. 1A and 1B, element 30, element 54, element 34-3 through 34-N; col 5, line 55 through col 6, line 3; col 6, line 52 through col 7, line 8. The trapping network (Fig. 1A, element 32) identifies packets to be recirculated when the compared destination addresses are equal and are not sent to the output port controller via the Banyan network. The outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} are packets not sent if the destination is not available for the packets. The packets are placed into shift registers (element 52) forming the recirculation loops (Fig. 1A, element 30) for later transmission when destination is reachable. Note: A shift register in the recirculation loop is a storage mechanism

coupled to the control logic to indicate whether the destination is reachable over the particular path).

Regarding Claim 23, Giacopelli et al. discloses an apparatus for forwarding information over a plurality of paths, the apparatus comprising:

a buffer to store a first set of packets (Fig. 1A, element 52; col 6, lines 63-66. A shift register for queuing is a recirculation buffer to store packets);

a random index generator to generate a random index (Fig. 1A, element 12, Fig. 2; col 4, line 43 through col 5, line 30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains two sub-fields, service priority field (SP) and switch priority (PR) (a count of number of time slots packet has been delayed). The Batcher network 12 is a random index generator to generate a random index based on the sorting of the SP and PR fields which is a random process);

an input to receive a second set of packets (Fig. 1A , element 16-M+1(input port controller); col 4, lines 28-42);

a set of switching logic coupled to the buffers and the plurality of paths (Fig. 1A , 1B, Fig. 6, element 80 (conflict resolution and routing); col 9, lines 39-49. The conflict resolution and routing device is a set of switching logic consisting of elements 12 (Batcher network), element 32 (trap cell network), element 36 (concentrator), element 38 (selector cell network) and elements 14a, 14b (Banyan network) and is coupled to

the recirculation buffer (element 52 via loop 30), random index generator (Batcher network), the set of paths (Banyan network) and the input (input port controller)); and control logic coupled to the buffer, the random index generator, the set of switching logic, and the input (Fig. 1A , 1B, Fig. 6, element 80 (conflict resolution and routing); col 9, lines 39-49. The conflict resolution and routing device is a control logic consisting of elements 12 (Batcher network), element 32 (trap cell network), element 36 (concentrator), element 38 (selector cell network) and elements 14a, 14b (Banyan network) and is coupled to the recirculation buffer (element 52 via loop 30), random index generator (Batcher network), the set of paths (Banyan network) and the input (input port controller));

wherein during a packet time, the control logic attempts to forward each packet of the first set of packets through the switching logic over each of the plurality of paths each packet time (Fig. 1A, 1B, elements 12 (Batcher network), element 32 (trap cell network), element 36 (concentrator), element 38 (selector cell network) and elements 14a, 14b (Banyan network); The packets arriving either from the input port controllers or recirculation path are processed using the control logic elements for forwarding to the output port controllers via the Banyan network each packet switching cycle (See col 4, line 43 through col 7, line 25));

wherein the switching logic determines a particular path of the plurality of paths for a particular packet in the first set of packets based on the random index (Fig. 1(element 12) and Fig. 2; col 5, lines 3-30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains

two sub-fields, service priority field (SP) and switch priority (PR). Sorting the SP and PR (a count of number of time slots packet has been delayed) fields is equivalent to the switching logic determining a particular path of the plurality of paths for a particular packet based on the random index which is provided by the randomness of both the service priority and switch priority of the packets);
and the control logic adds one or more packets from the second set of packets to replace packets sent from the first set of packets (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated. The selector cell network (element 38) based on the processed information of the packets (determined from the Batcher network, trap cell network and concentrator) forward the packets from the recirculation path to the output port controllers upon availability of transmission path in the Banyan network).

Regarding Claim 24, Giacopelli et al. discloses wherein a particular packet of the first set of packets is not sent during the packet time if a destination of the particular packet is not reachable over its corresponding the particular path (Fig. 1A and 1B, element 30, element 54, element 34-3 through 34-N; col 5, line 55 through col 6, line 3; col 6, line 52 through col 7, line 8. The trapping network (Fig. 1A, element 32) identifies packets to be recirculated when the compared destination addresses are equal and are not sent to the output port controller via the Banyan network. The outputs from selector

cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} are packets not sent if the destination is not available for the packets).

Regarding Claim 25, Giacopelli et al. discloses comprising a storage mechanism coupled to the control logic to indicate whether the destination is reachable over the particular path (Fig. 1A and 1B, element 30, element 54, element 34-3 through 34-N; col 5, line 55 through col 6, line 3; col 6, line 52 through col 7, line 8. The trapping network (Fig. 1A, element 32) identifies packets to be recirculated when the compared destination addresses are equal and are not sent to the output port controller via the Banyan network. The outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} are packets not sent if the destination is not available for the packets. The packets are placed into shift registers (element 52) forming the recirculation loops (Fig. 1A, element 30) for later transmission when destination is reachable. Note: A shift register in the recirculation loop is a storage mechanism coupled to the control logic to indicate whether the destination is reachable over the particular path).

Regarding Claim 26, Giacopelli et al. discloses an apparatus comprising: means for buffering a set of items, said set of items including a first set of items and a second set of items (Fig. 1A (element 54), Fig. 1B (element 18); col 3, lines 36-50; col 5, lines 31-37; col 6, line 52 through col 7, line 8). The first set of items are associated with selector cells (element 38, 40-1 through 40-N) outputs e_{1b},...a_{Nb} transmitted to the

Banyan networks 14a, 14b for routing to particular output port controller. The second set of items are associated with outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} to inputs a_1,..a_m forming the recirculation loops (Fig. 1A, element 30). Buffering of first set of items and second set of items occur in Fig. 1A (element 54), Fig. 1B (element 18));

means for forwarding the first set of items over a set of paths in a first configuration (Fig. 1A and 1B, col 5, lines 31-37. Connection path h1 to p1 to output port 18-1 from Banyan network 14a is associated with forwarding the first set of items over a set of paths in a first configuration);

means for reconfiguring the set of paths into a second configuration (Fig. 1A and 1B, col 5, lines 31-37. Connection path l1 to q1 to output port 18-1 from Banyan network 14b is associated with reconfiguring the set of paths into a second configuration); and

means for forwarding one or more items in the second set of items over the set of paths in the second configuration (Fig. 1A and 1B, col 5, lines 31-37; col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers and packets to be recirculated. The second set of items related to packets that have been recirculated, when identified by the trapping network to be routed to the output port controllers, is associated with forwarding one or more items in the second set of items over the set of paths in the second configuration).

Regarding Claim 27, Giacopelli et al. discloses means for placing the second set of items in a recirculation buffer (Fig. 1A and 1B, element 30 and element 54; col 6, line

52 through col 7, line 8. The second set of items are associated with outputs from selector cells (element 38, 40-1 through 40-N) designated as e_{1a}, ...e_{Ma} placed into shift registers (element 52) forming the recirculation loops (Fig. 1A, element 30). Note: A recirculation buffer is equivalent to a shift register in the recirculation loop); and means for retrieving said one or more items in the second set of items from the recirculation buffer (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers and packets to be recirculated. The recirculated packets placed in the shift register (element 52) when identified by the trapping network to be routed to the output port controllers is equivalent to retrieving one or more items in the second set of items from the recirculation buffer).

Regarding Claim 28, Giacopelli et al. discloses means for identifying the status of said paths (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 3; col 5, line 55 through col 6, line 6. A trap bit in the packet is set if the compared destination addresses are equal and the packet is to be recirculated. The trap bit is not set if the compared destination addresses are not equal and the packet is to exit to an output port controller via a banyan network 14. Setting the trap bit to determine if the packet is to be recirculated or transmitted to an output port controller via a Banyan network 14 is associated with identifying the status of paths).

Regarding Claim 29, Giacopelli et al. discloses an apparatus comprising:

means for identifying a random index (Fig. 1(element 12) and Fig. 2; col 5, lines 3-30. For packets addressed to the same destination, the Batcher network 12 will continue to sort over the priority field. The priority field contains two sub-fields, service priority field (SP) and switch priority (PR) (PR is a count of number of time slots packet has been delayed) fields. The switch priority (PR) is identified to be a random index);

means for determining whether the first particular packet can be sent over a first particular path of a plurality of paths, the first particular path identified based on the random index and a path occupancy (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 2, Fig. 3; col 5, lines 3-30; col 5, line 55 through col 6, line 6. The trap cell uses a comparator circuit to determine whether a particular packet can be sent over a particular path of a plurality of paths, the particular path identified based on the random index (switch priority (PR)) and a path occupancy (activity bit (A). Note: activity bit when set to "0" represents idle packet (recirculated packet) and when set to "1" is active packet (exiting packet equivalent to path occupancy))); and

means for causing said first particular packet to be sent over the first particular path or to remain in the recirculation buffer based on the result of said determining whether the first particular packet can be sent (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated); and

means for determining whether a second particular packet of a second set of received packets can be sent over a second particular path of a plurality of paths, the second particular path identified based on the random index and the path occupancy (Fig. 1A

and 1B, element 32 (trap cell, 34-3 through 34-N), Fig. 2, Fig. 3; col 5, lines 3-30; col 5, line 55 through col 6, line 6. The trap cell uses a comparator circuit to determine whether a particular packet can be sent over a particular path of a plurality of paths, the particular path identified based on the random index (switch priority (PR)) and a path occupancy (activity bit (A). Note: activity bit when set to "0" represents idle packet (recirculated packet) and when set to "1" is active packet (exiting packet equivalent to path occupancy))); and

means for causing said second particular packet to be sent over the second particular path or to remain in the recirculation buffer based on the result of said determining whether the second particular packet can be sent (Fig. 1A and 1B, element 32 (trap cell, 34-3 through 34-N); col 6, 24-31. The trapping network (Fig. 1A, element 32) identifies packets to be routed to the output port controllers or to be recirculated).

Regarding Claim 30, Giacopelli et al. discloses wherein the path occupancy is determined based on a number of paths over which the first particular packet or the second particular packet is caused to be sent in a current packet time (Fig. 6, Fig. 7, col 9, line 52 through col 10, line 40. All newly arriving packets at each input port controller are delayed for a period in excess of one packet slot. This provides time for an input port controller to decide in time slot T if it will be idle during the time slot T+2. If an input port controller will be idle during time slot T+2, then it serves as an access point for a recirculating packet. In such a case, the input port controller submits an active steering packet to the concentrator 92 that will be paired with a recirculating packet to provide a

routing header that returns the recirculating packet to the input port controller that issued the steering packet. The input port controller that receives the recirculating packet, will then resubmit the recirculating packet to the network 82 in the T+2 time slot. An input port controller that will not be idle during the packet time slot T+2 generates an idle steering packet during the packet slot T as indicated by an activity bit being set to zero. This process is equivalent to packet sent in a current packet time).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Giacopelli et al. (U.S. Patent No. 4,893,304) in view of Karol (U.S. Patent No. 5,416,769).

Regarding Claim 11, Giacopelli et al. discloses a packet switch architecture that is built around a Batcher sorting network and a plurality of banyan routing networks combining both internal queuing (i.e. recirculation) and output queuing (i.e. multiple paths to each output) that meets all the limitations of claims 1 through 10.

Giacopelli et al. does not disclose a computer-readable medium containing computer-executable instructions for performing the method of claim 1. Karol in the same field of endeavor discloses a computer-readable medium containing computer-executable instructions for performing the method of claim 1 (A control (Fig. 1, element 104) reads the header of packets at the inputs (element 101-1 to 101-n), controls the switching block (element 102) and recirculation lines (element 105-1 to 105-m) as suggested by Karol may be implemented on a microprocessor which executes programming instructions to perform the functions. See col 3, lines 10-55). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Giacopelli et al. to include such a control unit as taught by Karol for flexibility and efficiency in determining which packets need to be buffered in the recirculation delay lines and scheduling the delivery of the buffered packets based on their priority level (col 2, lines 8-12).

Regarding Claim 19, Giacopelli et al. discloses a packet switch architecture that is built around a Batcher sorting network and a plurality of banyan routing networks combining both internal queuing (i.e. recirculation) and output queuing (i.e. multiple paths to each output) that meets all the limitations of claims 12 through 18. Giacopelli et al. does not disclose a computer-readable medium containing computer-executable instructions for performing the method of claim 12. Karol in the same field of endeavor discloses a computer-readable medium containing computer-executable instructions for performing the method of claim 12 (A control (Fig.

1, element 104) reads the header of packets at the inputs (element 101-1 to 101-n), controls the switching block (element 102) and recirculation lines (element 105-1 to 105-m) as suggested by Karol may be implemented on a microprocessor which executes programming instructions to perform the functions. See col 3, lines 10-55). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the system of Giacopelli et al. to include such a control unit as taught by Karol for flexibility and efficiency in determining which packets need to be buffered in the recirculation delay lines and scheduling the delivery of the buffered packets based on their priority level (col 2, lines 8-12).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 4,866,701 to Giacopelli et al. relates to an architecture for a packet switch, and, more particularly, to a packet switch which dynamically allocates inputs between newly arriving packets and recirculating packets.

U. S. Patent No. 5,440,553 to Widjaja et al. relates to an output-buffered packet switch that has a plurality of inputs and outputs, implements a hybrid of shared and dedicated buffering, uses distributed architecture, provides priority transmission, guarantees packet sequence, is expandable, and can serve as a central control for a packet switch of higher speed.

U.S. Patent No. 5,636,210 to Agrawal relates to modular asynchronous transfer mode packet switch allowing expansion of the switch to handle applications having less than eight input and output devices to applications having up to 2^{14} input and output devices.

U.S. Patent No. 5,367,520 to Cordell relates to an ATM switch which is input buffered, employs a multiplicity of crosspoint switch planes operating simultaneously in parallel, and whose outputs are combined by an output-buffered second stage.

U.S. Patent No. 5,544,160 to Cloonan et al. relates to a physically realizable one terabit or more ATM packet switch that has a large number of input interfaces connected to a single stage switching fabric which is in turn connected to a number of output modules, generally according to the growable packet switch architecture with a single stage switch fabric controlled by an out-of-band controller.

U.S. Patent No. 5,856,977 to Yang et al. relates to a switch which includes at least one parallel distribution network with an NxN first routing network for receiving cells at a plurality of input ports. The routing network is self-routing and non-blocking, such as a Banyan Network.

The above prior art are cited to further show the same field of endeavor with respect to the applicant's claimed invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to F. Lin Khoo whose telephone number is 571-272-5508. The examiner can normally be reached on flex time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ajit Patel
Primary Examiner